In the Claims:

1. (currently amended) A leadframe for a semiconductor device, the leadframe comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter for receiving an integrated circuit die, wherein the inner perimeter of the paddle ring also includes a plurality of spaced projections;

a first row of terminals integral with, extending outwardly from, and generally surrounding the paddle ring, wherein the terminals of the first row of terminals are sized and shaped such that wires may be wirebonded between the terminals and bonding pads of an integrated circuit die disposed within the cavity and the terminals may be cut and thus separated from the paddle ring without destroying the wirebond;

a second row of terminals aligned with, surrounding and spaced from the first row of terminals; and

a connection bar surrounding the first and second rows of terminals, wherein each of the terminals of the second row of terminals is connected to the connection bar and wherein the first row of terminals is connected to the second row of terminals at a corner of the connection bar.

2. (original) The leadframe of claim 1, wherein the outer perimeter of the paddle ring includes a plurality of spaced projections.

3. (cancelled)

4. (original) The leadframe of claim 1, further comprising a paddle flag member located within the cavity that supports the integrated circuit die.

5. (original) The leadframe of claim 4, wherein the flag member is integral with the paddle ring.

6. (cancelled)

7. (cancelled)

8. (previously amended) The leadframe of claim 1, wherein the paddle ring is generally square shaped and the connection bar is connected to at least one of the terminals of the first row of terminals or the paddle ring at a corner thereof.

9. (previously amended) The leadframe of claim 8, further comprising another row of terminals connected to a first side of the connection bar opposing a second side of the connection bar to which the second row of terminals is connected, said another row of terminals for connecting to a second integrated circuit die.

10. (original) The leadframe of claim 1, wherein the leadframe is formed of copper.

11. (original) The leadframe of claim 10, wherein the leadframe is formed via an etching process.

12. (currently amended) A semiconductor device, comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter,

wherein the inner perimeter of the paddle ring also includes a plurality of spaced projections;

a first row of terminals integral with, extending outwardly from and generally surrounding the paddle ring, wherein each of the terminals of the first row of terminals is sized and shaped such that a wire may be wirebonded between the terminal and a bonding pad of an integrated circuit die disposed within the cavity and the terminal may be cut and thus separated from the paddle ring;

a second row of terminals aligned with, surrounding, and spaced from the first row of terminals;

a connection bar surrounding the first and second rows of terminals, wherein each of the terminals of the second row of terminals is connected to the connection bar and wherein the first row of terminals is connected to the second row of terminals at a corner of the connection bar;

an integrated circuit die placed within the cavity and surrounded by the paddle ring, the die including a plurality of die pads; and

a plurality of wires electrically connected to respective ones of the terminals of the first and second rows of terminals and the die pads.

13. (original) The semiconductor device of claim 12, further comprising:

a flag member located within the cavity that supports the integrated circuit die; and

an adhesive material layer disposed on a top surface of the flag member for securing the die to the flag member.

14. (original) The semiconductor device of claim 13, wherein the flag member is integral with the paddle ring.

15. (original) The semiconductor device of claim 12, further comprising an encapsulant covering a top surface of the integrated circuit die, the first and second rows of terminals, and the paddle ring, wherein at least a bottom surface of the first and second rows of terminals is exposed.

16. (cancelled)

17. (currently amended) The semiconductor device of claim 12~~16~~, wherein the outer perimeter of the paddle ring also includes a plurality of spaced projections.